POWER SUPPLY WITH CAPACITIVE MAINS ISOLATION

RELATED APPLICATIONS

[0001] The present application claims priority under 35 U.S.C. § 119 of Provisional Patent Application Serial Number 60/418,823 filed on October 16, 2002.

FIELD OF THE INVENTION

[0002] The present invention relates to power supplies in general, and more particularly, to generating a supply voltage using capacitive isolation.

BACKGROUND OF THE INVENTION

[0003] Power supplies serve the purpose of converting an input voltage into one or several output voltages. An AC power source may be used to provide an AC power line input, which gets converted to a DC regulated output voltage. Transformers are typically used to provide isolation for a power supply or a converter. However, transformers are typically large in size (due to the size of the magnetic elements within them), bulky and expensive devices. A regulated power supply that utilizes capacitive elements to transform an input voltage from an AC power source to a specified output voltage level across a load is desired.

SUMMARY OF THE INVENTION

[0004] A power supply with capacitive mains isolation, comprises a source of an input supply voltage developed between a first terminal and a second terminal. A first supply inductance is coupled to the first terminal, and a second supply inductance is coupled to a load circuit. A switch responsive to a periodic control signal applies the input supply voltage to the first supply inductance to generate a current in the first supply inductance at a first polarity, during a first portion of a period of the control signal when the switch is at a first switch state. A pair of capacitors operate to couple the first supply inductance to the second supply inductance during a second portion of the period of the control signal when the switch is at a second switch state. The pair of capacitors isolate the first and second terminals, respectively, from the second supply inductance at a range of frequencies that is lower than a frequency of the control signal. A first rectifier is coupled to the first supply inductance for preventing the first supply inductance current from changing polarity, during the second portion of the period.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figure 1 shows a power supply with capacitive mains isolation in accordance with an embodiment of the present invention.

[0006] Figure 2 shows waveforms associated with the operation of the circuit shown in Figure 1.

[0007] Figure 3 shows a standby power supply with capacitive mains isolation in accordance with another embodiment of the present invention.

[0008] Figure 4 shows a standby power supply with capacitive mains isolation including a mechanism for providing a lower output voltage in accordance with another embodiment of the present invention.

DETAILED DESCRIPTION

[0009] Figure 1 depicts an exemplary circuit arrangement 100 adapted to provide a power supply having capacitive mains isolation according to an embodiment of the present invention. An input supply voltage Vin is developed and applied at input node 10a of circuit 100. Inductor L1 and diode D1 are connected in series with one another, with L1 having a first terminal L1a connected to node 10a, and a second terminal L1b connected to the anode of diode D1. The cathode of diode D1 is connected at node 10b to terminal C1a of first isolation capacitor C1, whose second terminal C1b is connected to node 10c. Switch S1 selectively provides a direct path between node 10b and reference potential or ground (GND). Isolation capacitor C2 has a first terminal connected to GND and a second terminal connected to C1 through inductor L2. Capacitors C1 and C2 provide isolation due to the fact that the capacitors have a high impedance at the relatively low frequency of Vin. However, the capacitors represent a low impedance at the frequency of operation of switch S1, which is at a higher frequency than that of Vin. Switch S1 is responsive to a control signal 62 from control circuit 60 for selectively opening/closing the connection between node 10b and GND to disable/enable application of the input supply voltage Vin to inductor L1. In this manner the switch is operated at a given frequency f1 in accordance with the control signal. Capacitors C1 and C2 have low impedance with respect to this frequency. For example, capacitors C1 and C2 may have a low impedance in relation to operation of switch S1 at 50KHz, while providing a high impedance and isolation at an input voltage Vin of, for example 50Hz or 60Hz. While switch S1 is shown as a simple switch, it is

understood that various implementations are possible, such as one or more switching transistors, relays, solenoids, and the like.

[0010] Still referring to Figure 1, diode D2 is connected between nodes 10c and 10d, while load RL and filter capacitor C3 are connected in parallel between nodes 10d and 10e. Isolation capacitor C2 has a first terminal C2a coupled to GND, and a second terminal C2b coupled to node 10e. Inductor L2 is connected between node 10c and 10e. Node 10e is connected to a second reference or isolated ground potential gnd2.

[0011] Operation of power supply circuit 100 is described with reference to Figure 1 in conjunction with the respective waveforms shown in Figure 2. Initially (i.e. time t0), switch S1 is closed ("on") to cause current I(L1) to rise linearly and store energy in inductor L1. At the same time a sinusoidal current I(L2) begins to transfer the stored energy of C1 and C2 to L2. When the voltage across capacitor C1 exceeds the output voltage (Vout) at time t1, diode D2 conducts and the energy in inductor L2 is transferred to capacitor C3. Note that between time t0 and time t1, current flows in the path of circuit elements L2, C1, S1 and C2 (in the counterclockwise direction). At time t1, the path of current changes to flow in the clockwise direction through circuit elements L2, D2 and C3. This is because the voltage across C1 and C2 equals the voltage across C3 (i.e. Vout). At time t2, S1 is switched "off" (i.e. opened). Current I(L1) continues to flow through the circuit elements D1, C1, D2, C3 and C2 back to the mains until the energy stored in L1 is transferred to C1, C2 and C3. At time t2, current I(L1) slightly increases due to the condition that Vin is higher than the voltage V(S1) at node 10b. During this energy transfer, diode D1 embodying an inventive feature is conducting in the forward direction. As soon as the current in L1 drops to zero at time t3 (due to resonance with C1, C2, C3) diode D1 changes to a non-conductive state and the current I(L1) is maintained at zero. A flow back of energy from C1, C2 back to L1 (oscillation) is thereby advantageously suppressed. Diode D1 advantageously increases the efficiency of the circuit since the entire energy is thereby stored in C1 and C2. Diode D1 allows the use of a free-running oscillator for controlling S1. At time t4, the energy in L2 is completely transferred into C3. The time interval between t4 and t5 is a "dead time" and can be varied to regulate the transfer of power between the input and output terminals. Note that when S1 is again turned "on" (e.g. at time t5), current I(L1) again rises linearly, and the above described sequence is repeated.

[0012] Figure 3 illustrates an exemplary embodiment of a standby power supply having capacitive mains isolation according to the present invention. A control unit U1 such as a standard SMPS controller, is connected between nodes 10b and GND via terminals U1d and U1g, respectively, and further includes a supply terminal U1a and feedback terminal U1b. U1a is the supply terminal where the internal supply voltage of the integrated circuit (internal to U1) is developed. More particularly, the supply terminal U1a is energized internally in the IC in a manner not shown. Bypass capacitor C4 is connected between supply terminal U1a and GND for providing power from integrated circuit U1, while terminal U1b is connected to coupler U2, which may be an opto-coupler, for example. In an exemplary embodiment, control unit U1 operates at a constant frequency, such as 50 Kilohertz (50 KHz) and includes an internal startup or initialization circuit. Voltage regulation is realized by operating the control unit in an on/off mode or burst mode. When the output voltage Vout exceeds the voltage reference level of Zener diode D4 which is connected to secondary ground gnd2 by resistor R1, the controller is switched off via opto-coupler U2. A decreasing output voltage turns the controller on again. Note that L2 can be provided with a tap T as shown in Figure 4, in the event that a second, lower output voltage is desired. As illustrated in the embodiment of Figure 4, tap T is connected to inductor L2, and to capacitor C4 via diode D5 to secondary ground gnd2. Note that the output voltage VLS is provided by the ratio of the turns of the inductor L2.

[0013] Although the invention has been described in terms of exemplary embodiments, it is not limited thereto. The appended claims should be construed broadly to include other variants and embodiments of the invention which may be made by those skilled in the art without departing from the scope and range of equivalents of the invention.